Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(previously presented) A process for filling a via hole in a layer of FSG, having an upper surface, comprising the sequential steps of:
depositing the layer of FSG on a substrate;
depositing a layer of USG on only the entire upper surface;
patterning and then etching only said USG and FSG layers, whereby a via hole, having walls and extending as far as the substrate, is formed;
depositing a seed layer on the walls of the via hole;
overfilling the via hole with a material; and
by means of CMP, removing said material until said USG layer is reached.

2.(original) The process described in claim 1 wherein the FSG layer is deposited to a thickness between about 0.2 and 1 microns and contains between about 3 and 10 atomic % fluorine.

3.(original) The process described in claim 1 wherein the USG layer is deposited to a thickness between about 0.1 and 0.2 microns and acts as an end-point detector during CMP.

4.(original) The process described in claim 1 wherein the step of depositing the USG layer further comprises using PECVD from silane or TEOS at about 400 °C.

5.(original) A process for forming a single damascene connector, comprising the sequential steps of:
providing a partially completed integrated circuit and then depositing thereon a layer of FSG having an upper surface;
depositing a layer of USG on said upper surface;
on the USG layer, depositing a layer of silicon oxynitride for use as an anti-reflection coating;
patterning and then etching said oxynitride, USG, and FSG layers, thereby forming a via hole extending as far as said integrated circuit;
depositing a barrier layer on all walls of the via hole;
depositing a copper seed layer on said barrier layer;

overfilling the via hole with copper; and
by means of CMP, removing the copper until said USG layer is reached, thereby forming said damascene connector.

6.(original) The process described in claim 5 wherein the step of depositing the USG layer further comprises using PECVD from silane or TEOS at about 400 °C .

7.(original) The process described in claim 5 wherein the USG layer is deposited to a thickness between about 0.1 and 0.2 microns.

8.(original) The process described in claim 5 wherein the step of removing the copper until said USG layer is reached further comprises optical detection of the USG layer through a change in reflectivity.

9.(original) A process for forming a dual damascene connector, comprising the sequential steps of:
providing a partially completed integrated circuit and then depositing thereon a layer of silicon nitride;
on said layer of silicon nitride, depositing a layer of FSG having an upper surface;
depositing a layer of USG on said upper surface;
on the USG layer, depositing a layer of silicon oxynitride for use as an anti-reflection coating;
patterning and then etching said oxynitride, USG, and FSG layers, thereby forming a trench in said upper surface;
patterning and then etching said FSG layer, including said trench, whereby a via hole extending as far as said layer of silicon nitride is formed inside said trench;
selectively removing the layer of silicon nitride;
depositing a barrier layer on all walls of said trench and said via hole;
depositing a copper seed layer on said barrier layer;
overfilling said via hole and said trench with copper; and
by means of CMP, removing the copper until said USG layer is reached, thereby forming said damascene connector.

10.(original) The process described in claim 9 wherein the layer of silicon nitride is deposited to a thickness between about 300 and 1,000 Angstroms.

11.(original) The process described in claim 9 wherein the layer of silicon oxynitride is deposited to a thickness between about 400 and 1,500 Angstroms.

12.(original) The process described in claim 9 wherein the step of removing the copper until said USG layer is reached further comprises optical detection of the USG layer through a change in reflectivity.

13.(withdrawn) A filled via hole in a layer of FSG, comprising:
said layer of FSG being on a substrate;
a layer of USG, having an upper surface, on the layer of FSG;
said via hole extending from said upper surface to the substrate; and
the via hole being filled with a material.

14.(withdrawn) The filled via hole described in claim 13 wherein the FSG layer is between about 0.4 and 1 microns thick and contains between about 3 and 10 atomic % fluorine.

15.(withdrawn) The filled via hole described in claim 13 wherein the USG layer is between about 0.1 and 0.2 microns thick.

16.(withdrawn) A single damascene connector, comprising:
a layer of FSG on a partially completed integrated circuit having a surface;
a layer of USG, having a first upper surface, on said layer of FSG;
a via hole extending from said first upper surface as far as the surface of the integrated circuit;
a barrier layer on all walls of the via hole; and
the via hole being filled with copper having a second upper surface that is flush with said first upper surface.

17.(withdrawn) The single damascene connector described in claim 16 wherein the barrier layer is selected from the group consisting of tantalum, tantalum nitride, titanium nitride, and titanium silicon nitride.

18.(withdrawn) The single damascene connector described in claim 16 wherein the barrier layer is between about 50 and 500 Angstroms thick.

19.(withdrawn) A dual damascene connector, comprising:
a layer of FSG on a partially completed integrated circuit having a surface;
a layer of USG, having a first upper surface, on said layer of FSG;
a trench, extending from said first upper surface through the USG layer a distance into the FSG layer, said trench having first sidewalls and a floor;
a via hole, having second sidewalls, extending from said trench floor through the FSG layer, as far as the surface of the integrated circuit;

a barrier layer on the first and second sidewalls and on the trench floor; and

the via hole and trench being filled with copper that has a second upper surface that is flush with said first upper surface.

20.(withdrawn) The dual damascene connector described in claim 19 wherein the trench has a width between about 0.1 and 1 microns and a depth between about 0.2 and 1 microns.

21.(withdrawn) The dual damascene connector described in claim 19 wherein the via hole has a width between about 0.1 and 0.6 microns and a depth between about 0.4 and 1 microns.

22.(withdrawn) The dual damascene connector described in claim 19 wherein the USG layer is between about 0.1 and 0.2 microns thick.